Hardware Implementation of wavelet based Image encoder

Prashant R. Deshmukh

Department of Computer Science, Sipna College of Engg and Technology, Amaravati,India

pr_deshmukh@yahoo.com

S.A. Ladhake

Sipna College of Engg and Technology, Infront of Nemani Godown, Badnera road, Amaravati, India

G.G. Sarate

Department of Electronics Engg, P. R.M. Research and Technology, Badnera, India

ggs_anshu@rediffmail.com

ABSTRACT

Although FPGA technology offers the potential of designing high performance systems at low cost, its programming model is prohibitively low level. To allow a novice signal/image processing end-user to benefit from this kind of devices, the level of design abstraction needs to be raised. This approach will help the application developer to focus on signal/image processing algorithms rather than on low-level designs and implementations. This paper presents a framework for an FPGA-based Discrete Wavelet Transform system. The approach helps the end-user to generate FPGA configurations for DWT at a high level In this paper, the proposed DWT (Discrete Wavelet Transform) filter bank is made of simple architecture, but it is efficiently designed that a user have facility to provide desired compression rate. After implementation on FPGA chip, the designed encoder operates at 73.82MHz.

Categories and Subject Descriptors

B.6.3 [VHDL], H.2.O [Image]

General Terms

Performance, Design

Keywords

Wavelet, FPGA, Filter Bank

1   INTRODUCTION

Compression is based on two fundamental principles. One principle is to use the properties of signal source and to remove redundancy from the signal. When considering digital images as realizations of two-dimensional stochastic process, this structure manifests itself through statistical dependencies between pixels. The other principle is irrelevancy reduction that is to exploit the properties called human visual system that is not perfect and to omit parts or details of the signal that will not be noticed by the receiver[3].The theory of subband decomposition provides an efficient framework for the implementation of schemes for redundancy and irrelevancy reduction. It has been demonstrated repeatedly in subband and wavelet based schemes. The important motives of using subband decomposition schemes are the demand for a "scalable" image representation [8].

The subband image decomposition using wavelet transform has a lot of advantages. Generally, it profits analysis for non-stationary image signal and has high compression rate.

In this paper, it is implemented by FPGA using xilinx chip, after VHDL coding of DWT encoder for image processing. It uses filter bank pyramid algorithm for wavelet transform and can speed up as each filter consists of the FIR filter and two filters are connected with parallel structure that can compute lowpass and highpass DWT coefficients in the same clock cycle. Because of using QMF properties, it reduces half number of the multiplier needed DWT computation. It can increase efficiency as well as reduce hardware size. Also, a user can manipulate the designed encoder with input parameter control i.e. compression rate.

2   BACK GROUND THEORY

The last few years , wavelet transform has been widely used for wide range of multimedia applications including signal analysis, signal decoding, image processing and compression. Wavelet transform can be studied from mathematical point of view as a projection of a signal on the set of basis function [7] similarly to the Fourier transform . The difference is that , the basis in the Fourier transform are sine and cosines, are infinite, in contrary to the basis function of the wavelet transform that are finite .In wavelet analysis, signals are represented using a set of basis functions derived by shifting and scaling a single prototype function. The family of wavelet basis functions can be generated by translating and dilating the mother wavelet corresponding to the wavelet. Given a fixed scale m, one can find a "mother" scaling function (t) such that the family of functions

$$\phi_{mn}(t) = 2^{-m/2} \phi(2^{-m}t - n) \qquad (1)$$

forms a orthogonal basis. If $f_m(t)$ denotes the value of $f(t)$ at resolution level m, then $f_m(t)$ can be represented

$$f_m(t) = \sum c_{(m+1)n}\phi_{(m+1)n} + \sum d_{(m+1)n}\varphi_{(m+1)n} \qquad (2)$$

in this equation $c_{(m+1)n}$ and $d_{(m+1)n}$ are the scaling coefficients and the wavelet coefficients respectively. Mathematically expressed as

$$c_{mn} = \sum_{k} h(k-2n)c_{(m-1)k}$$

$$d_{mn} = \sum_{k} g(k-2n)d_{(m-1)k} \qquad (3)$$

$$g_{M-1-m} = (-1)^m h_m \quad (M > 2) \tag{4}$$

In equation 3 , h(z) and g(z) are low pass and high pass filter obtained from the wavelet. Therefore (*t*) is consider a low pass function and $\varphi(t)$ is considered as a band pass function , then the function can be synthesized as the sum of low and high frequency components where m is the resolution level. As shown in equation 4, the wavelet coefficients are obtained from alternating flip of scaling filter coefficients . Daunbechies satisfies this relation ship between the filter coefficients.

The short-time Fourier transform uses the same size of filter on the entire time-frequency domain, the wavelet transform takes different size of windows at variable scale, so that it is suitable to analyze spatial and spectral locality. Mallat showed that this multiresolution representation of a signal could be computed using a pyramid filter structure of quadrate mirror filter (QMF) pairs [7]. The implementation of the DWT can be realized in the form of filter banks [4]. Each filter bank comprises lowpass and highpass filters succeeded by decimation by two. In this paper Daubechies 4 wavelets algorithm is used for computing DWT coefficients. The filter coefficients is shown in table 1.

Table 1 : The daubenchies filter coefficients

N	H	G
0	0.48296291314453	0.12940952255126
1	0.83651630373781	0.22414386804201
2	0.22414386804201	-0.83651630373781
3	-0.12940952255126	0.48296291314453

If we apply equation 4 to the low pass and high pass filter , the transfer function H(z) and G(z) can be rewritten

$$H(z) = h_0 + h_1 Z^{-1} + \dots\dots + h_{M-1} Z^{-(M-1)}$$

$$G(z) = (-1)^{M-1} h_{M-1} + (-1)^{M-2} h_{M-2} h_1 Z^{-1} + \dots\dots + (-1)^0 h_0 Z^{-(M-1)}$$

$$\tag{5}$$

As shown in equation 3, the DWT computation is rather complex because of the data dependencies at different stage . Fig 1 shows data flow diagram of DWT computation in DWT filter. The 4 tap Daubenchies can be computed as follows :

$$H_n = h_0 a_{2n} + h_1 a_{2n-1} + h_2 a_{2n-2} + h_3 a_{2n-3} \quad \text{:Low}$$

$$G_n = -h_3 a_{2n} + h_2 a_{2n-1} - h_1 a_{2n-2} + h_0 a_{2n-3} \quad \text{:High}$$

$$\tag{6}$$

$$H_0 = h_0 a_0$$

$$G_0 = -h_3 a_0$$

$$H_1 = h_0 a_2 + h_1 a_1 + h_2 a_0$$

$$G_1 = -h_1 a_0 + h_2 a_1 - h_3 a_2 \quad \dots\dots \quad \& \text{ so on}$$

$$\tag{7}$$

3   ARCHITECTURE :

The proposed DWT encoder in this paper processes input 8 bit data that is original image. Greatly, it consists of two blocks, i.e. filter bank and controller. In addition to them, normalization is used to normalized image as desired for filter bank, whereas coefficient register holds filter coefficients during read/write access operation. The controller that monitors the separated read and write address counter for RAM read/write operation, receives parameter value and controls overall system and data/address selector, which selects read/write addresses of the separated RAM.

The process for the highpass and lowpass DWT coefficient computation can obtain from filter bank that consists of simple FIR filter with adder and multiplier as shown in Fig.2. The adder and multiplier used FIR filter makes use of 18-bit floating point , consisting of 11 bit mantissa and 6-bit exponent and 1 bit reserved as a sign bit. Fig.3 represents DWT filter block diagram.
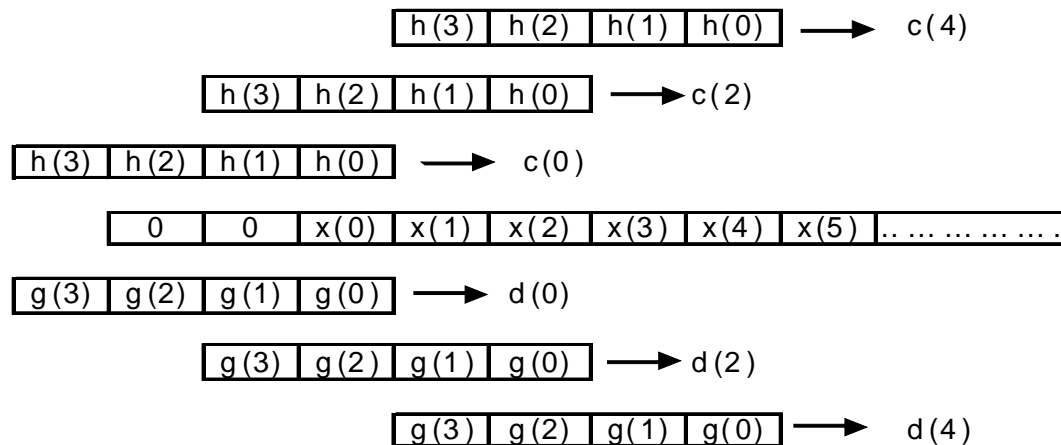
F ig 1 . Data Flow diagram
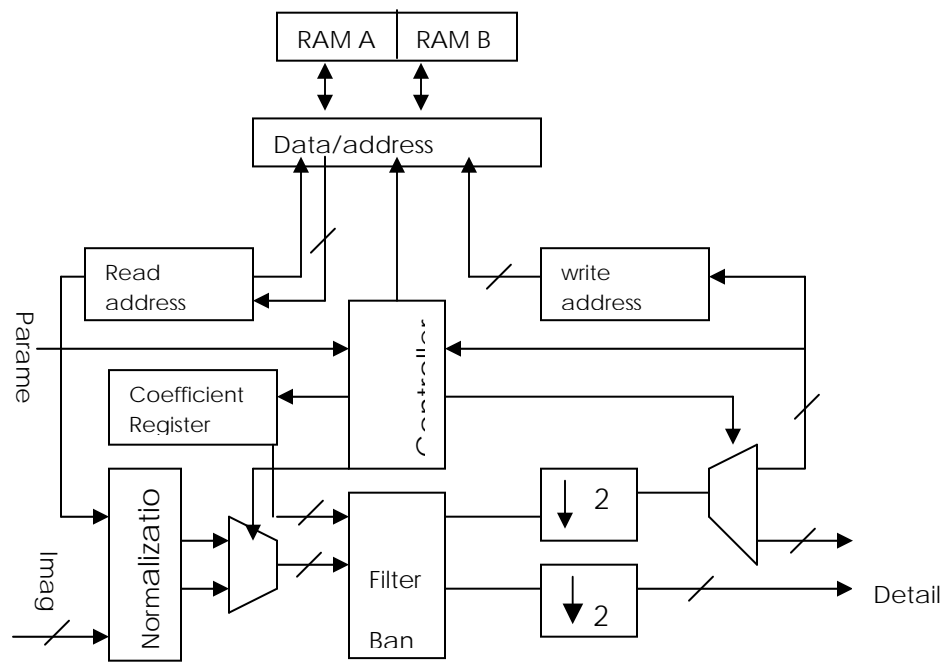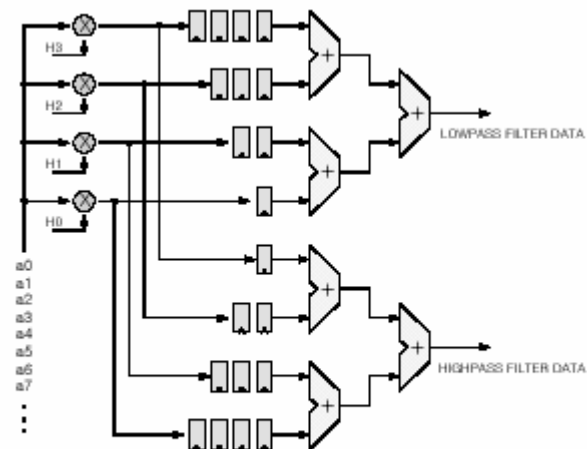
Fig. 2 Block diagram
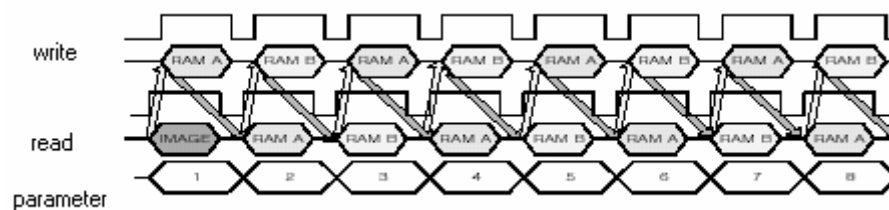

Fig. 3. DWT filter bank

Fig 4 Memory Aceess Timing cycles

The input data feeds in the multiplier that has parallel structure for high speed processing without delay. After converting sign bit (Eq.4), the output data through the multiplier feeds in a part of delay using floating-point advantages for highpass and lowpass DWT coefficients computation. The signal through out lowpass filter is an important bit more than a point to reconstruct original signal because it is $\sqrt{2}$ times. The signal through out highpass filter is an less important bit than point to reconstruct original signal because it approaches near zero. If the proposed encoder is designed by fixed-point arithmetic, it requires additional control circuit to identify the point location. A floating-point expression of number can extend expressible range. Each filter composed different coefficients of filter bank can multiply without special care. Therefore, users can control it easily and obtain the multiplied result with high precision. Fig 4. is expressed separated memory accessed cycles corresponding to the input parameter.

The output data from the DWT filter bank is stored in RAM pointed by address counter. For computing two dimension DWT, however, read operation is complex. After finishing write operation of processing present data, read address counter increase address for loading data. Due to down sampling, the Clock cycle of output data from the DWT Filter Bank is twice as small as the system clock cycle. RAM basically consist of two RAMS to do read and write operation simultaneously just to speed the operation. . The processed average signal results out through DEMUX corresponding to input parameter.

4   CONCLUSION :

In this paper, the proposed DWT encoder can increase efficiency and users obtain a desired compression rate through input parameter. The proposed designs have been functionally checked for an 512*512 image (Leena) by simulating the VHDL code on a Model sim simulator and synthesized using synplicity tool. While synthesized against xilinx Spartan-II FPGA target device , the operating frequency for proposed architecture is found around 73.82 MHz, & it uses 659 CLB's(Configurable logic Blocks). It can be possible to process to max 10 stages(input parameter) on xilinx Spartan-II FPGA target device. Same can be increased by targeting over different target device such as Xilinx VirtexII, Altera(Flex10k-50),Lattice etc.

5   REFERENCE :

[1] A.Grzeszczak, M.K.Mandal, "VLSI Implementation of Discrete Wavelet Transform", IEEE Transactions on VLSI System, Vol.4, No.4, pp 421-433, Dec 1996.

[2] A. S. Lewis and G. Knowles, ``Image compression using the 2-D wavelet transform," IEEE Trans. on Image Processing, vol. 1, no. 2, pp. 244-250, April 1992.

[3] G. Knowles, ``VLSI architecture for the discrete wavelet transform," Electron. Lett., vol. 26, no. 15, pp. 1184-1185, July 1990.

[4] Gilbert Strang/Truong, "Wavelet and Filter Bank",Wellesley-Cambridge Press, 1996. [7]. Ali N.Akansu, Mark J.T.Smith, "Subband wavelet transforms design and application", Kluwer academic publishers. 1996

[5] K. Parhi and T. Nishitani, ``VLSI architectures for discrete wavelet transform," IEEE Trans. on VLSI Systems, vol. 1, no. 2, p p. 191-202, 1993.

[6] M. Vishwanath, R. M. Owens, ``VLSI Architectures for the discrete wavelet transform," IEEE Trans. on Circuits and Systems, vol. 42, pp. 305-316, May 1995.

[7] Mallat ,"Wavelet Tour of signal processing ", Academic press, second edition ,1999.

[8] Rafael C. Gonzalez, Richard E. Woods "Digital Image Processing" Addison-wesley publishing company, 1993 This research is supported by IDEC at KAIST, 2002, Korea

Author's biography

Prashant R. Deshmukh is working as a Professor and Head. He has total teaching experience of 20 years. He did his B.E. in 1988, M.E. in 1995 and PhD in 2005. His area of interest is VLSI, Microprocessor/Microcontrollers. He is members of various professional societies such as ISTE, IEEE, IE, IETE,ISIO etc. He has to his credit more than 55 publications in National and International Conference proceedings and Journals.

S.A. Ladhake is working as Pricnipal. He has 24 years of experience ion field of Teaching and Industry. He did his PhD in field of Analog design in 2003. He is promoter and Chairman of IETE centre at Amravati. His area of interest is analog design , signal processing. He is He is members of various professional societies such as ISTE, IEEE, IE, IETE etc. He has to his credit more than 25 publications in National and International Conference proceedings and Journals.

G.G.Sarate was born in 1967 in Akola, Maharashtra, India. He received his BE Electronics, ME Electronics degrees from Amravati University Amravati in the years 1990 and 1998 respectively. He completed his Ph.D. in Optical Fiber Devices in 2006. He has worked as Lecture in Electronics in B. N. College of Engg. Pusad Dist. Yavatmal for four years. Presently he is working as Professor in Electronics & Telecommunication Engg. at Prof. Ram Meghe Institute of Technology & Research Badnera, Amravati. He has to his credit more than 27 publications in National and International Conference proceedings and Journals.